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Pipeline Template for Streaming Applications on Heterogeneous Chips

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Abstract. We address the problem of providing support for executing single streaming applications implemented as a pipeline of stages that run on heterogeneous chips comprised of several cores and one on-chip GPU. In this paper, we mainly focus on the API that allows the user to specify the type of parallelism exploited by each pipeline stage running on the multicore CPU, the mapping of the pipeline stages to the devices (GPU or CPU), and the number of active threads. We use a real streaming application as a case of study to illustrate the experimental results that can be obtained with this API. With this example, we evaluate how the different parameter values affect the performance and energy efficiency of a heterogeneous on-chip processor (Exynos 5 Octa) that has three different computational cores: a GPU, an ARM Cortex-A15 quad-core, and an ARM Cortex-A7 quad-core.

Keywords. Parallel Pipeline, Heterogeneous chips, On-chip GPU, Performance-Energy efficiency

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